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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/471,435	12/23/1999	MICHAEL J. MCTAGUE	INTL-0296-US	7390

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TIMOTHY N TROP
TROP PRUNER HU & MILES PC
8554 KATY FREEWAY
SUITE 100
HOUSTON, TX 77024

EXAMINER
TRAN, KHANH C

ART UNIT	PAPER NUMBER
2631	

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Please find below and/or attached an Office communication concerning this application or proceeding.

HG

PR4

Office Action Summary	Application No. 09/471,435	Applicant(s) MCTAGUE ET AL.	
	Examiner Khanh Tran	Art Unit 2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-10 & 14-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. U.S. Patent 6,345,072 B1.

Regarding claims 1 and 14,

- Liu et al. discloses, in figure 2A, a DSL modem 200 configured on the motherboard with two physically separated circuitry sections, a DSL modem analog circuit 205, and a DSL modem digital circuit 230, to improve noise performance in the analog front end section.
- Figure 2B (sheet 2) shows a detailed DSL modem analog circuit 205 including an A/D converter 213. Liu et al's invention is to support any type of high speed DSL modem (e.g. ADSL modem).
- Figure 1A shows a previous configuration of prior art supporting V.90 type of modem, said configuration including a Voice Band Modem digital circuitry 130 and a Voice Band Modem analog circuitry 110. Data transmits/and receives over slow data lines SDATA_IN (serial, time division multiplexed input data stream to the PC) and SDATA_OUT (serial,

time division multiplexed output data stream from the PC). Liu et al.'s teachings further discuss that when oversampling is used in A/D and D/A, the digital filters for interpolation and decimation filters can be done on either side of the DSL link. Hence, a decimation filter is required in the receive path in figure 2B (sheet 2), containing said A/D converter 213, to produce lower data rate for said link SDATA_IN in figure 1A and an interpolation filter is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', to increase the sampling rate of data received on SDATA_OUT in figure 1A to support faster DSL mode in Liu et al.'s invention.

- Liu et al. further discusses the receive and/or transmit signal lines can also be used for carrying control words for use by the DSL modem, which controls words are embedded as part of the normal data stream. Hence, a multiplexer is required in the receive path in figure 2B (sheet 2), containing said A/D converter 213, for multiplexing data and control words and transmitting said multiplexed data out on SDATA_IN in figure 1A. A demultiplexer is also required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', for demultiplexing serialized data received on SDATA_OUT in figure 1A. From all discussion above, combining prior art with Liu et al's invention would have been obvious to one of ordinary skill in the art.

Regarding claim 2, as recited in claim 1, said multiplexed data on SDATA_IN in figure 1A is received by a DSL Modem digital circuitry 230 in figure 2B (sheet 1). It would have been obvious that a demultiplexer is required in said DSL Modem digital circuitry 230 for demultiplexing the multiplexed data for further processing.

Regarding claims 3 and 15, as recited in claim 1 above, a decimation filter is required to lower the sampling rate of the A/D converter 213 for transmitting externally.

Regarding claim 4, figure 2B shows an analog filter 211 coupled to the A/D converter 213. It would have been obvious said decimation filter replacing a digital filter 214 and said multiplexer coupled to said decimation filter.

Regarding claim 5, as recited in claim 1, a demultiplexer is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', for demultiplexing multiplexed data received on SDATA_OUT in figure 1A.

Regarding claims 6, 20 and 21, as recited in claims 1 and 5, an interpolation filter is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', to increase the sampling rate of data received on SDATA_OUT in figure 1A to support faster DSL mode as taught by Liu et al.'s invention.

Regarding claim 7, Liu et al. shows in figure 2B the analog section includes both the receive and transmit paths.

Regarding claim 8, Liu et al. shows in figure 2A a DSL modem including a DSL modem digital circuitry 230 having a receive section 234 coupled to receive multiplexed data on SDATA_IN in figure 1A.

Regarding claim 9, it would have been obvious that said DSL modem digital circuitry 230 can implement discrete multi-tone modulation.

Regarding claim 10, Liu et al. teaches in figure 2A, lines 30-48, a DSL Modem Digital Circuit 230 may be implemented in a single integrated circuit chip and also includes circuitry for performing some of necessary digital signal processing.

Regarding claim 16, as recited in claims 14 and 15, Liu discloses the receive and/or transmit signal lines can also be used for carrying control words for use by the DSL modem, which controls words are embedded as part of the normal data stream. It would have been obvious that a multiplexer is required in the receive path in figure 2B (sheet 2), containing said A/D converter 213, for multiplexing data and control words and transmitting said multiplexed data out on SDATA_IN in figure 1A.

Regarding claim 17, Liu et al. shows in figure 2A a DSL modem including a DSL modem digital circuitry 230 having a receive section coupled to receive multiplexed data from the DSL analog digital circuitry 205. It would have been obvious that a demultiplexer is required in said DSL Modem digital circuitry 230 for demultiplexing the multiplexed data for further processing.

Regarding claim 18, as recited in claim 1, the digital filters for interpolation and decimation filters can be done on either side of the DSL link when oversampling is done in the A/D and D/A converters. Therefore, an interpolation filter is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', to increase the sampling rate of data received on SDATA_OUT in figure 1A to support faster DSL mode as taught by Liu et al.'s invention.

Regarding claim 19, in column 7, lines 30-40, Liu et al. discloses that DSL functions (such as IFFT and FFT) could be performed by 234' and 234, respectively.

Regarding claim 22, figure 2B shows a D/A converter 213'.

Regarding claim 23, -

Liu et al. discloses, in figure 2A, a DSL modem 200 configured on the motherboard with two physically separated circuitry sections, a DSL modem analog circuit 205, and a DSL modem digital circuit 230, to improve noise performance in the analog front end section.

- Figure 2B (sheet 2) shows a detailed DSL modem analog circuit 205 including an A/D converter 213. Liu et al's invention is to support any type of high speed DSL modem (e.g. ADSL modem).

- Figure 1A shows a previous configuration of prior art supporting V.90 type of modem, said configuration including a Voice Band Modem digital circuitry 130 and a Voice Band Modem analog circuitry 110. Data transmits/and receives over slow data lines SDATA_IN (serial, time division multiplexed input data stream to the PC) and SDATA_OUT (serial, time division multiplexed output data stream from the PC). Liu et al.'s teachings further discuss that when oversampling is used in A/D and D/A, the digital filters for interpolation and decimation filters can be done on either side of the DSL link. Hence, a decimation filter is required in the receive path in figure 2B (sheet 2), containing said A/D converter 213, to produce lower data rate for said link SDATA_IN in figure 1A and an

interpolation filter is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', to increase the sampling rate of data received on SDATA_OUT in figure 1A to support faster DSL mode in Liu et al.'s invention.

- Liu et al. further discusses the receive and/or transmit signal lines can also be used for carrying control words for use by the DSL modem, which controls words are embedded as part of the normal data stream. Hence, a multiplexer is required in the receive path in figure 2B (sheet 2), containing said A/D converter 213, for multiplexing data and control words and transmitting said multiplexed data out on SDATA_IN in figure 1A. A demultiplexer is also required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', for demultiplexing serialized data received on SDATA_OUT in figure 1A. From all discussion above, combining prior art with Liu et al's invention would have been obvious to one of ordinary skill in the art.

- Said multiplexed data on SDATA_IN in figure 1A is received by a DSL Modem digital circuitry 230 in figure 2B (sheet 1). It would have been obvious that a demultiplexer is required in said DSL Modem digital circuitry 230 for demultiplexing the multiplexed data for further processing.

Regarding claim 24, claim 11 recites a QAM decoding block 112 included in the receiver of said DSL modem digital circuit 230. It would have been obvious that a QAM encoder is employed in the transmit path for encoding fast DSL data and a decimation

filter is required to lower data rate, a serializer is required for converting data serially and transmitting out on SDATA_OUT in figure 1A. As recited in claim 1, the digital filters for interpolation and decimation filters can be done on either side of the DSL link when oversampling is done in the A/D and D/A converters. Therefore, an interpolation filter is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', to increase the sampling rate of data received on SDATA_OUT in figure 1A to support faster DSL mode as taught by Liu et al.'s invention.

Regarding claim 25, as recited in claim 23, a decimation filter is included in a DSL modem analog circuit 205 for lowering the sampling rate of the A/D converter 213.

Regarding claim 26, as recited in claim 24, an interpolation filter is required in the transmit path in figure 2B (sheet 2), containing a D/A converter 213', to increase the sampling rate of data received on SDATA_OUT in figure 1A to support faster DSL mode as taught by Liu et al.'s invention.

Regarding claim 27, as recited in claim 13, in column 7, lines 30-40, Liu et al. teaches that DSL functions (such as IFFT and FFT) can be performed by 234' and 234 in figure 2B (sheet 1).

Regard claim 28, it would have been obvious the DSL modem as taught by Liu et al. can be easily implemented as splitterless and can be installed remotely.

Regarding claim 29, as recited in claim 23, Liu discloses the receive and/or transmit signal lines can also be used for carrying control words for use by the DSL modem, which controls words are embedded as part of the normal data stream. It would have been obvious that a multiplexer is included in the DSL modem analog circuit 205

for multiplexing data and control words and transmitting them to the DSL modem digital circuitry 237 in figure 2B (sheet 1).

Regarding claim 30, figure 1A shows a modem, supporting V.90, including data lines, SDATA_OUT and SDATA_IN in both directions.

2. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al. U.S. Patent 6,345,072 B1 as applied to claims 1, 8 and 9 above, and further in view of Cheng et al. U.S. Patent 6,456,650 B1.

Regarding claim 11, claims 1, 8 and 9 recite limitations of claim 11 above. Furthermore, Cheng et al. discloses in figure 3 a DSL receiver includes a Fast Fourier Transform block 110, a Quadrature Amplitude Modulation (QAM) decoding block 112. It would have been obvious that various modifications can be implemented in said DSL modem digital circuit 230 as taught by Liu et al.; therefore, a combination of Cheng et al. and Liu et al.'s teachings would have been obvious for one of ordinary skill in the art.

Regarding claim 12, claim 11 recites a QAM decoding block 112 included in the receiver of said DSL modem digital circuit 230. It would have been obvious that a QAM encoder is employed in the transmit path for encoding fast DSL data and a decimation filter is required to lower data rate, a serializer is required for converting data serially and transmitting out on SDATA_OUT in figure 1A.

Regarding claim 13, in column 7, lines 30-40, Liu et al. teaches that DSL functions (such as IFFT and FFT) can be performed by 234' and 234 in figure 2B (sheet 1).

Conclusion

3. The prior art made of record and not relied upon could be considered pertinent to applicant's disclosure:

Norsworthy et al. U.S. Patent 5,512898 discloses a data converter.

Koizumi et al. U.S. Patent 6,393,051 B1 discloses a DSL communicating system and a transceiver in the system.

Isaksson et al. U.S. Patent 6,456,649 B1 discloses multi-carrier transmission systems.

Langberg et al. U.S. Patent 6,421,377 B1 discloses a system and method for ech cancellation over asymmetric spectra.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 703-305-2384. The examiner can normally be reached on Monday - Friday from 08:00 AM - 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 703-305-4378. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3800.

KCT
September 27, 2002

CHI PHAM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600 10/1/02